AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Claims 1 - 107 (Cancelled)

108. (Previously Presented) A method of forming an interconnect structure, comprising:

forming a first dielectric layer on a substrate;

removing a portion of the first dielectric layer;

forming a second dielectric layer on the substrate where the portion of the first dielectric layer was removed; and

forming a plurality of signal lines in the first dielectric layer and a power line in the second dielectric layer.

109. (Currently Amended) The method of claim 108, wherein a dielectric constant of the first dielectric layer is different from a dielectric constant of the second dielectric layer.

110. (Previously Presented) The method of claim 109, wherein forming the plurality of signal lines and the power line comprises etching trenches in the first and the second dielectrics, depositing a conductive material, and polishing the conductive material such that the conductive material is substantially removed except for that which is in the trenches.

Claim 111 (Cancelled)

112. (Previously Presented) A microelectronic device comprising an interconnect structure formed by the method of claim 108.

Claims 113-122 (Cancelled)

123. (New) The method of claim 108, wherein the dielectric constant of the first dielectric layer is lower than the dielectric constant of the second dielectric layer.

124. (New) A microelectronic device comprising an interconnect structure formed by the method of claim 123.

125. (New) The method of claim 123:

wherein the dielectric constant of the first dielectric layer is lower than that of silicon dioxide; and

wherein the dielectric constant of the second dielectric layer is greater than or equal to that of silicon dioxide.

126. (New) The method of claim 125, wherein the first dielectric layer comprises an organic polymer.

127. (New) The method of claim 125, wherein the first dielectric layer comprises a silicon based insulator containing an organic polymer.

128. (New) The method of claim 125, wherein the first dielectric layer comprises a nanofoam.

129. (New) The method of claim 125, wherein the first dielectric layer comprises a fluorine doped oxide of silicon.

130. (New) The method of claim 125, wherein the dielectric constant of the second dielectric layer is greater than that of silicon dioxide.

131. (New) The method of claim 130, wherein the second dielectric layer comprises barium strontium titinate.

132. (New) The method of claim 108, further comprising after forming the first dielectric layer on the substrate, and prior to removing the portion of the first dielectric layer, forming a patterned masking layer over the first dielectric layer.

133. (New) The method of claim 108, wherein forming the second dielectric layer comprises planarizing a material of the second dielectric layer.

134. (New) The method of claim 133, wherein planarizing the material comprises chemical-mechanical polishing the material.

135. (New) The method of claim 108, wherein forming the first and the second interconnect lines comprises forming the interconnect lines by a damascene process.

136. (New) The method of claim 135, wherein forming the plurality of signal lines in the first dielectric layer comprises etching trenches in the first dielectric layer, depositing a conductive material, and polishing the conductive material to remove a portion which is not in the trenches.

137. (New) A method comprising:

forming a first dielectric layer on a substrate;

removing a portion of the first dielectric layer;

forming a second dielectric layer on the substrate where the portion of the first dielectric layer was removed; and

forming a first interconnect line in the first dielectric layer and a second interconnect line in the second dielectric layer.

138. (New) A microelectronic device comprising an interconnect structure formed by the method of claim 137.

139. (New) The method of claim 137, wherein the first dielectric layer comprises a higher dielectric constant than the second dielectric layer, and wherein the first interconnect line comprises a power line and the second interconnect line comprises a signal line.

140. (New) A microelectronic device comprising an interconnect structure formed by the method of claim 139.

141. (New) The method of claim 139:

wherein the dielectric constant of the first dielectric layer is greater than or equal to that of silicon dioxide; and

wherein the dielectric constant of the second dielectric layer is lower than that of silicon dioxide.

142. (New) The method of claim 143, wherein the second dielectric layer comprises an organic polymer.

143. (New) The method of claim 143, wherein the second dielectric layer comprises a silicon based insulator containing an organic polymer.

144. (New) The method of claim 143, wherein the second dielectric layer comprises a nanofoam.

145. (New) The method of claim 143, wherein the second dielectric layer comprises a fluorine doped oxide of silicon.

146. (New) The method of claim 143, wherein the dielectric constant of the first dielectric layer is greater than that of silicon dioxide.

147. (New) The method of claim 148, wherein the first dielectric layer comprises barium strontium titinate.

148. (New) The method of claim 137, wherein the second dielectric layer comprises a higher dielectric constant than the first dielectric layer, and wherein the second interconnect line comprises a power line and the first interconnect line comprises a signal line.

149. (New) A microelectronic device comprising an interconnect structure formed by the method of claim 148.

150. (New) The method of claim 137, further comprising after forming the first dielectric layer on the substrate, and prior to removing the portion of the first dielectric layer, forming a patterned masking layer over the first dielectric layer.

151. (New) The method of claim 137, wherein forming the second dielectric layer comprises planarizing a material of the second dielectric layer.

152. (New) The method of claim 137, wherein planarizing the material comprises chemical-mechanical polishing the material.

153. (New) The method of claim 137, wherein forming the first and the second interconnect lines comprises forming the interconnect lines by a damascene process.